Google

static timing circuit merge results mode corner

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1. System and method for providing distributed **static timing** analysis ...

   by K Kucukcakar - 2005
   A **static timing** analysis tool can advantageously manage multiple runs having different modes and **corners** and automatically **merge** the **results** generated by **...**
   www.freepatentsonline.com/y2005/0172250.html

2. 6 STATISTICAL **STATIC TIMING**

   static timing analysis (STA) runs at the process **corners**, a more **.....** Experimental **results** on benchmark **circuits** show that these bounds are very **...** sal, using the bound to **merge** groups of arrival times when possible, and thus **...**
   www.springerlink.com/index/q3117762611678O8.pdf - Similar

3. Magma - Quartz **Time**

   It provides the most sophisticated **static timing** and signal integrity analysis technology **...** Multi-**mode** timing analysis allows concurrent analysis and optimization of **...** Quartz Time's multi-**corner** timing analysis generates timing constraints that **...** TSMC Selects FineSim Pro **Circuit** Simulator to Develop Analog IP **...**
   www.magma-da.com/products-solutions/analysis/quartz**time**.aspx - Cached

4. Archive | DAC Proceedings

   We report **results** based on OCP benchmarks for a 672 processors with NOC **.....** Solving one such reported node in worst **corner** will resolve multiple violations. **....** The increasing number of **corners** and modes raises the possibility of cross **mode** setup-hold conflict **.... Static Timing** Analysis of Single Track **Circuits ...**
   www.dac.com/events/proceedings.aspx?id=95-5-U - Cached - Similar

5. [PDF] Z **CIRCUIT**

   File Format: PDF/Adobe Acrobat - View as HTML
   corner or not taking advantage of a special operating voltage, may lead to a **...** specific model **results** and simulations, if a problem is detected. **...** single-step **mode** allows the user to rapidly identify problems in **circuit** behavior. **... Static Timing** Analysis. SI Analysis. Power Estimation. Place & Route **...**
   www.z-**circuit**.com/CharDatasheet04_18.pdf

6. Statistical **static timing** analysis: A survey - Elsevier

   by C Forzan - 2009 - Related articles - All 3 versions
   Typically, the methodology to determine the **circuit timing** performance spread under variability is to run multiple **static timing** analyses (STA) at different **...**
   linkinghub.elsevier.com/retrieve/pii/S0167926008000564

7. **Circuit** and method for modeling I/O - US Patent 6983432 Description

   6, the **static timer** can **merge** on-chip and off-chip **timing**, perform signal **...** The spice run **results** are merged with **static timing** assertions by the **static ...**
   www.patentstorm.us/patents/6983432/description.html

8. Gate Sizing Using Incremental Parameterized Statistical **Timing ...**

   by MR Guthaus - 2005 - Cited by 65 - Related articles
   This paper uses incremental, parametric statistical **static timing** analysis (SSTA) to perform gate sizing with a required **...** is defined for early **mode** timing analysis. **Corner**-based DSTA **.....** ities as they **merge** into their respective sink timing points. **....** produces sub-par **results** on many **circuits**. This work has **...**
   ieeexplore.ieee.org/iel5/10431/33130/01560213.pdf?arnumber=1560213

9. [PDF] Timing Yield Estimation Using Statistical **Static Timing** Analysis

   File Format: PDF/Adobe Acrobat - Quick View
   by M Pan - Cited by 7 - Related articles
   Conventional deterministic **static timing** analysis handles variability by analyzing a **circuit** at multiple process **corners**. Although this method **...**
   www.eecs.northwestern.edu/~haizhou/publications/iscas05.pdf

10. [PDF] AccuCore **Static Timing** Analysis

    File Format: PDF/Adobe Acrobat
    timing of a digital **circuit** without requiring simulation. **.....** ß The use of **corners** in **static timing** analysis has several limitations **...**
    www.simucad.com/products/ip.../AccuCore_Static_Timing.pdf

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static timing circuit merge results mode corner coverage

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1. System and method for providing distributed **static timing** analysis ...

   by K Kucukcakar - 2005
   A **static timing** analysis tool can advantageously manage multiple runs having different modes and **corners** and automatically **merge** the **results** generated by **...**
   www.freepatentsonline.com/y2005/0172250.html

2. USER TRACK - DAC Archives

   Getting sufficient Functional **Coverage** in a timely manner is a **...** In this poster, we present the **results** of our experience developing and using a generic CDC verification flow. **.....** with some blocks of partitions under MMMC (Multi-**Mode** Multi-**Corner**) condition. **....** **Static Timing** Analysis of Single Track **Circuits ...**
   www.dac.com/events/eventdetails.aspx?id=95-5-U - Cached - Similar

3. Statistical **Static Timing** Analysis - A Better Alternative EDA ...

   By Rakesh Chadha, J. Bhasker, eSilicon Traditionally **static timing ...** at a **corner** which **results** in max delay and the METAL2 is at the **corner** which **results** in min delay. **...** If +/- 2.576σ **coverage** is selected, the statistical distribution meets **...** Computer Aided Design of Microwave **Circuits** (Artech House, 1981). **...**
   www.scribd.com/.../Statistical-**Static**-**Timing**-Analysis-A-Better-Alternative-EDA-DesignLine - Cached

4. [PDF] Implementing an End-to-End Low-Power Multi-Voltage Methodology

   File Format: PDF/Adobe Acrobat - Quick View
   when the **circuit** is active (dynamic power) and also when it is inactive (static power). **.....** later in the design flow can avoid

equivalence **coverage** problems and **.... Static timing** analysis is based on two delay components: the network **...** Concurrent Multi-**Corner** and Multi-**Mode** (MCMM) Analysis and Optimization **...**
www.synopsys.com/Solutions/EndSolutions/.../implement_wp.pdf

5. Magma: Talus RTL

   Fast, Accurate **Static Timing** Analysis • Hierarchical timing constraints • Timing reports and graphical timing analyzer • Multi-**mode** analysis **...**
   www.magma-da.com/products-solutions/.../talusrtl.aspx - Cached

6. ETD Search **Results**: "More Like This" Search

   For example, the **corner**-to-**corner** interconnect delay of a xc2v8000 FPGA is about **....** Multiple functions are obtained on a single Boolean **static** logic **circuit ...** A variety of current and voltage **mode** threshold logic gates implemented in **...** (maximum frequency) or the place and route **time** for the overall **circuit**. **...**
   etd.ohiolink.edu/search.cgi?q=accession_number...mlt=y - Cached

7. [PDF] AccuCore **Static Timing** Analysis

   File Format: PDF/Adobe Acrobat
   so it may not give broad **coverage** of the **circuit .....** ß The use of **corners** in **static timing** analysis has several limitations ß It may be overly optimistic **...**
   www.simucad.com/products/ip.../AccuCore_**Static_Timing**.pdf

8. Microsoft PowerPoint - ChanduVisweswariahISSCC04v10

   by C Visweswariah - Cited by 12 - Related articles - All 3 versions
   would require 220 **timing** runs to hit all **corners**. – cumbersome, risky and pessimistic all at the same **...** What is a statistical **timer**? **Static timer**. Delay and slew models. Netlist **.....** in a **circuit** with 1M nodes and 2M edges and 12 **timing ....** Test **coverage** can be improved by exploiting statistical **timing results ...**
   domino.research.ibm.com/.../ChanduVisweswariahISSCC04v10.PDF

9. **Timing** analysis with compact variation-aware standard cell models **...**

   by SA Aftabjahani - 2009 - Cited by 2 - Related articles - All 4 versions
   The **results** demonstrate improved accuracy in comparison with table-based static **...** The standard approach to estimate **circuit** timing is through **static timing ...** The "**corner**" models consist of tables relating delay and output slew to **.....** to the eigenvectors selected for the model determine the variance **coverage**. **...**

linkinghub.elsevier.com/retrieve/pii/S0167926008000710 - Similar

10. FAQ

It uncovers difficult to reach **corner** cases and provides a guarantee that **...** Solidify's **static coverage** technology guides the designer to create a **.... time** and effort since only those unverified portions of the **circuit** are analyzed. **...**
www.averant.com/faq.html - Cached

1 2 3 4 5 6 7 8 9 10 Next

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static timing circuit unanalyzed results mode corner coverage

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1. COMPELLING GOVERNMENTAL INTERESTS: AN ESSENTIAL BUT **UNANALYZED** ...

by SE GOTTLIEB - 1988 - Cited by 131 - Related articles

The logical **result** of this approach mandated a change, because, as defined, **....** at the same **time**, the rejection of unlisted rights confined the **.....** 277 In each **mode** of analysis, the benefits of a particular definition of rights **.....** 1 (1955) (contending that the draftsmen did not intend a **static** meaning of **...**

https://litigation-essentials.lexisnexis.com/.../app?...1...

2. User interface having analysis status indicators - US Patent ...

The magnet 22 creates a **static** magnetic field alongthe longitudinal axis of **....** The uppermost left-hand **corner** contains an indication 46 of the computer program being run. **...** the computer analyzed visual image and the **unanalyzed** visual image. **...** Once in cinema **mode**, the user can scroll rapidly through an entire **...**

www.patentstorm.us/patents/7155043/description.html

3. [PDF] NP-complete Problems and Physical Reality

File Format: PDF/Adobe Acrobat - View as HTML

by S Aaronson - Cited by 59 - Related articles - All 20 versions

In general, the **results** were highly nondeterministic; I could obtain **.....** evolving dynamically in **time**: instead there is just a **static** spacetime **....** since we can simulate the classical **time** travel **circuit** for PSPACE using a quantum **circuit**. On **....** should we treat the user who picks an input x as an **unanalyzed**, **...**

www.scottaaronson.com/papers/npcomplete.pdf - Similar

4. Method and Apparatus for Video Digest Generation - Patent application

[0184]Abbreviation **mode** (15A) **results** in a video digest with both large duration and covering. The main emphasis is on showing the

content in less **time**, ...
www.faqs.org/patents/app/20090022472 - Cached

5. [PDF] DELAYING WITH FIRE: THE SHEARON HARRIS NUCLEAR PLANT AND 14 YEARS ...

File Format: PDF/Adobe Acrobat - View as HTML
stress at **corners** and in narrow openings; and electrical loads. **....** high number of **circuit** failures can occur in a relatively short **time** period, in that case within **.... unanalyzed** manual actions. 1. Fire Watch Patrols **.....** Information Notice 2005-07, "**Results** of HEMYC Electrical Raceway Fire Barrier System Full **...**
www.nowarn.org/.../WP%20DELAYING%20W%20FIRE%20REP.pdf - Similar

6. SIGACT News Complexity Theory Column 46

by S Aaronson - 2005 - Cited by 59 - Related articles
Complexity; Subhash Khot on Recent **results** in PCPs and Hardness of **.....** evolving dynamically in **time**: instead there is just a **static** spacetime **....** I am indebted to Lance Fortnow for coming up with a **time** travel **circuit** for the more general **....** should we treat the user who picks an input x as an **unanalyzed**, **...**
portal.acm.org/ft_gateway.cfm?id=1052804&type=pdf

7. <a href="http://arXiv.org/abs/quant-ph/0502072v2">arXiv:quant-ph ...

by S Aaronson - 2005 - Cited by 59 - Related articles - All 20 versions
Feb 21, 2005 **...** In general, the **results** were highly nondeterministic; **.....** not even a notion of objects evolving dynamically in **time**: instead there is just a **static** spacetime **....** since we can simulate the classical **time** travel **circuit** for **....** should we treat the user who picks an input x as an **unanalyzed**, **...**
arxiv.org/pdf/quant-ph/0502072

8. (WO/2009/035764) METHOD AND APPARATUS FOR VIDEO DIGEST GENERATION

Figure 16 illustrates non-linear **time** warp for preview generation. **...** playback of various **time** portions of a previously **unanalyzed** input media content **.....** or (for relatively **static** objects) may be done without first determining that the **.....** Abbreviation **mode** (15A) **results** in a video digest with both large **...**
www.wipo.int/pctdb/ja/ia.jsp?ia=US2008%2F070224&IA... - Cached

9. [PDF] V. ARCHEOLOGICAL ASSESSMENT

File Format: PDF/Adobe Acrobat - View as HTML
surveys, however, vary in intensity of **coverage** and detail of recording. **....** can vary, ranging from recognition of (1) the material **results** of a single **.....** are materials from other excavations that are also **unanalyzed**. **....** Most of the **time**, archeologists work with the assumption of

static ahupua'a boundaries **...**
www.nps.gov/havo/historyculture/upload/HAVO_AOA_part%203.pdf

10. Stanford Computer Science Department Technical Reports from the 1970s

The computation **time** is proportional to V^3, where V is the number of vertices; **.....** such information for the case in which the model is an edge or **corner**. **.....** These **circuits** have one **mode** of operation called secure **mode** in which they **.....** whose performance in many cases remains **unanalyzed**, is Shellsort. **...**
infolab.stanford.edu/TR/cstr7x.html - Cached - Similar

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Results **1** - **10** of about **65,900** for **static timing circuit violation path coverage report interface user input**. (**0.09** seconds)

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1. Replicating timing data in **static timing** analysis operation

At least one **path** comprising logical **user** defined delay segments and a **timing ...** Many of the common problems in chip design relate to **interface timing ...** For instance, the **input** data may vary, and/or the **circuit** may perform **...** Examples of problems that can occur from poor **timing** include a hold **time violation**, **...**
www.freshpatents.com/-dt20091126ptan20090293031.php - Cached

2. Concurrently modeling delays between points in **static timing ...**

An apparatus, program product and method perform **static timing** analysis on an **...** Many of the common problems in chip design relate to **interface** timing **...** For instance, the **input** data may vary, and/or the **circuit** may perform **...** Examples of problems that can occur from poor timing include a hold time **violation**, **...**
www.freshpatents.com/-dt20091126ptan20090293030.php - Cached

3. **Static timing** analysis - Wikipedia, the free encyclopedia

A hold **time violation**, when an **input** signal change too quickly, **...** Once the **circuit timing** has been computed by one of the techniques below, the critical **...** in most of the literature on **timing** analysis refers to the critical **path** method **...** Many of the common problems in chip designing are related to **interface ...**
en.wikipedia.org/wiki/Static_timing_analysis - Cached - Similar

4. Method and apparatus for analyzing digital **circuits** - US Patent **...**

Static timing analysis tools have the capability to verify **circuit** timings more **...** SCSI host bus adapter 112, and expansion bus **interface** 114 are connected to PCI **...** Otherwise, the process **reports violations** identified in step 210 (step 214) **...** Glitch **path** 520 begins at the set **input** of latch 518 and traces back **...**
www.patentstorm.us/patents/5903577/description.html

5. [PDF] **Static Timing** Verification of Custom Blocks Using Synopsys ...

   File Format: PDF/Adobe Acrobat - View as HTML

   a particular sensitization leads to a **timing violation** in the **circuit** block. **....** of the **reports** generated by NanoTime also look similar to those generated by PrimeTime. **.....** **path** from a design **input** (referred to as a source) to a design output or **timing .....** Faster runtime, an interactive **user interface** and a **...**

   www.synopsys.com/Tools/Implementation/SignOff/.../nano_wp.pdf

6. Method and timing harness for system level **static timing** analysis ...

   by RWL Ko - 2008 - All 4 versions

   May 13, 2008 **...** Method for performing timing analysis of a clock-shaping **circuit ....** 16 illustrates an example of a timing **report** generated by a **....** of tracing and correcting timing **violations** compared to previous methods of I/O boundary analysis. **....** An "internal **path**" approach was proposed in "**Static Timing ...**

   www.freepatentsonline.com/7373626.html

7. Focus **Report**: **Timing** Analysis - EETimes.com | Electronics Industry ...

   Furthermore, **static timing** tools automatically guide the **user** to the most critical **... path** is intentional, it must be specified to avoid a hold **violation**. **...** rather than exhaustive **coverage** of every **circuit** node in the design. **...** then links them into timing-analysis tools using the OLA modeling **interface**. **...**

   www.eetimes.com/editorial/2000/focus**report**0008.html - Cached - Similar

8. [PDF] Chapter 7: **Timing** Constraints for HardCopy II Devices

   File Format: PDF/Adobe Acrobat - View as HTML

   Quartus II software, an **interface** to a third-party **static timing** analyzer, **....** in the Compilation **Report** and resolve all reported timing **violations**. Constraining **....** In combinational timing **circuits**, a **path** exists from a primary **input** port **...** translations produce the same timing constraint **coverage** and the same **...**

   www.altera.com/literature/hb/hrd/hc_h51028.pdf - Similar

9. [PDF] Open Verilog international

   File Format: PDF/Adobe Acrobat - Quick View

   to the use of PrimeTime, the Synopsys **static timing** analysis. (STA) tool. **....** To invoke the shell: To invoke the PrimeTime shell as an alternative **user interface**, execute: **...** does not **report** non-cell **violations**, e.g. output **path violations ...** creates timing paths and **reports** rising edge **input** timing and **...**

   www.eas.uccs.edu/cileti/.../Tutorials/prime**time**_tut.pdf

10. Strategic **Timing** Analysis of High-speed Boards - IEEE Spectrum

by LL Chang - 1997 - Cited by 1 - Related articles

Many tools are available for **static timing** analysis on ICs and **circuit** boards. But **....** if there are no more timing **violations**. A false **path** that has timing **violations** will be reported by Motive. **....** Defining Terms) or a **user** script. Here, only the tool **..... input**, should see a low signal at its **input** pin sooner **...**

ieeexplore.ieee.org/iel3/6/12503/00576012.pdf?arnumber=576012

1 2 3 4 5 6 7 8 9 10 Next

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1. **Static timing** analysis - Wikipedia, the free encyclopedia

   A hold **time violation**, when an **input** signal change too quickly, **...** Once the **circuit timing** has been computed by one of the techniques below, the critical **...** in most of the literature on **timing** analysis refers to the critical **path** method **...** Many of the common problems in chip designing are related to **interface ...**
   en.wikipedia.org/wiki/**Static_timing**_analysis - Cached - Similar

2. Method and timing harness for system level **static timing** analysis **...**

   The **input** delay is set to constrain a setup/hold timing requirement on an **...** A virtual clock has no real source inthe integrated **circuit** design **.....** An "internal **path**" approach was proposed in "**Static Timing** Verification of **.....** The timing **report** may be used for analysis and correction of timing **violations**. **...**
   www.patentstorm.us/patents/7373626/description.html

3. Focus **Report**: **Timing** Analysis - EETimes.com | Electronics Industry **...**

   Furthermore, **static timing** tools automatically guide the **user** to the most critical **... path** is intentional, it must be specified to avoid a hold **violation**. **...** rather than exhaustive **coverage** of every **circuit** node in the design. **...** then links them into timing-analysis tools using the OLA modeling **interface**. **...**
   www.eetimes.com/editorial/2000/focus**report**0008.html - Cached - Similar

4. CommsDesign - Overcoming **Static Timing** Issues in Low-Power 3G Chips

   But, while cutting power, these tricks can create **static timing** analysis problems. **...** As a result, the **input** clock cannot be used as a timing reference for **...** For each **interface**, reference the **interface's** I/O timing assertions to **...** The first pass updates timing and **reports** the insertion delay of the I/O clocks. **...**
   www.commsdesign.com/design_corner/showArticle.jhtml?... - Cached

5. [PDF] Save **Time** and Money with CustomSim Native **Circuit** Checks

   File Format: PDF/Adobe Acrobat - View as HTML

   programmable **interface**. Often, it has only been possible to check for certain failure mechanisms by **....** paths between two **user**-defined power supplies. The check will **report** DC paths as **...** analyze the native **circuit** check **violation report**. **...** through increased error **coverage** utilizing high-speed **static** checks in **...**

   www.synopsys.com/Tools/.../CircuitSimulation/.../Custom-Circuit-wp.pdf - Similar

6. Strategic **Timing** Analysis of High-speed Boards - IEEE Spectrum

   by LL Chang - 1997 - Cited by 1 - Related articles

   functional simulation starts at 0 **percent**, **static** tim- **...** if there are no more **timing violations**. A false **path** that has **timing ...** built either directly, from the **circuit** board schemat. **....** Defining Terms) or a **user** script. Here, only the tool **.....** **input**, should see a low signal at its **input** pin sooner than U5. **...**

   ieeexplore.ieee.org/iel3/6/12503/00576012.pdf?arnumber=576012

7. **Static** Netlist Verification

   A graphical **user interface** (GUI) for easier debugging **....** results from a given **input** without any timing **violations**. The problem with dynamic timing analysis is that the simulation vectors cannot guarantee 100 **percent coverage**. **Static timing** analysis checks all the paths in the **circuit** or design, including the **...**

   www.springerlink.com/index/r5g27651q1670ln6.pdf

8. **Coverage** Metrics for Functional Validation of Hardware Designs

   by S Tasiran

   In this article, we summarize existing work on coverage metrics, **report** on **....** is to ask for **user input**, but this approach may be **time** consuming and error prone. **...** As with code coverage, **circuit**-structure-based metrics provide a lower **...** These metrics require state, transition, or limited **path coverage** on a **...**

   doi.ieeecomputersociety.org/10.1109/54.936247

9. [PDF] **Coverage** Metrics for Functional Validation of Hardware Designs

   File Format: PDF/Adobe Acrobat - Quick View

   by S Tasiran - Cited by 91 - Related articles - All 23 versions

   age metrics, **report** on industrial experiences in **....** toggle coverage: Each binary node in the **circuit ...** mon solution is to ask for **user input**, but this approach may be **time** consuming and error **...** state, transition, or limited **path coverage** on a **....** coverage, therefore, is the **percentage** of faults **...**

   citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.62.9086&rep...

10. Patent Issued Week 16, 2009

The method can include receiving a **user input** request to voice-enable at least **...** A method for propagating phase constants for **static circuit** model analysis is provided. **...** clock pairs in order to minimize cycle-**time** overlap **violations ...** A computer system includes a user-**interface**. The user-**interface** includes a **...**
www.freepatentsonline.com/ISD-04142009-p2.html

1 2 3 4 5 6 7 8 9 10 Next

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Results **1** - **10** of about **56,800** for **static timing circuit violation path results mode corner coverage**. (**0.09** seconds)

Show options...

1. Statistical **Static Timing** Analysis - A Better Alternative EDA ...

Timing analysis at the traditional interconnect **corners** considers various **...** SSTA **Results** The **results** from statistical analysis provide **path** slack in terms **...** Assuming -/+3σý' **coverage**, the effective minimum value has a **violation** by 0.12ns **path ...** Computer Aided Design of Microwave **Circuits** (Artech House, 1981). **...**
www.scribd.com/.../Statistical-Static-Timing-Analysis-A-Better-Alternative-EDA-DesignLine - Cached

2. Embedded.com - Statistical **Static Timing** Analysis - A Better ...

Feb 3, 2009 **...** Statistical **static timing** analysis (SSTA) helps the design team **...** The **results** from statistical analysis provide **path** slack in terms of its mean and **corner** values. **...** If +/- 2.576σ **coverage** is selected, the statistical distribution **...** 0.5% of the manufactured parts will have a timing **violation**. **...**
www.embedded.com › Design Articles - Cached

3. Statistical **Static Timing** Analysis - A Better Alternative

Traditionally **static timing** analysis (STA) is used to verify if a CMOS digital **...** is at a **corner** which **results** in max delay and the METAL2 is at the **corner ...** Assuming -/+3ω **coverage**, the effective minimum value has a **violation** by 0.12ns - **path ...** Computer Aided Design of Microwave **Circuits** (Artech House, 1981). **...**
www.chipestimate.com/techtalk.php?d=2008-12-30 - Similar

4. METHODS FOR CONSERVING MEMORY IN STATISTICAL **STATIC TIMING** ...

A method for memory conservation during statistical **static timing** analysis **...** integrated **circuit** timing based on statistical **static timing** analysis. **...** slack or an early **mode** slack indicates a timing constraint **violation**. **.....** Patents in all subclasses Timing analysis (e.g., delay time, **path** delay, latch timing) **...**
www.faqs.org/patents/app/20090241078 - Cached

5. SCDsource - Expert's **Corner** - Who needs statistical **timing** and how **...**

   You want to check the timing of the **circuit** everywhere in the process space. **...** Reason number two is full chip **coverage**. If you do things on a **path** basis, **...** Does it completely replace multi-**corner static timing** analysis, or complement **...** are not just timing **violations** you have to fix, but robustness **violations**, **...**
   www.scdsource.com/experts.php?id=5 - Cached - Similar

6. System and method for correlated process pessimism removal for **...**

   Static timing is used widely in order to verify the **timing** of digital **.....** In the elucidatory **circuit** of FIG. 3, BOX340 in the late data **path** and BOX320 in **...**
   www.patentstorm.us/patents/7117466/description.html

7. Chip Design » **Static Timing** Analysis at 28 nm: More and Bigger is **...**

   For over 10 years, design engineers have used the same **static timing ... circuit** designers to predict speed, timing and power of their sensitive. **...** View **Results ...** and distributed multi-**mode**/multi-**corner** (MM/MC) and location-based on-chip **...** where an ECO that fixes the original timing **violation** creates another. **...**
   chipdesignmag.com/display.php?articleId=3790 - Cached

8. USER TRACK - DAC Archives

   In this poster, we present the **results** of our experience developing and using a generic CDC verification flow. **..... Static Timing** Analysis of Single Track **Circuits ...** This verification flow enables timing-**violation**-driven ECO flows of **...** how false and multi-cycle **path** information from **Static Timing** Analysis **...**
   www.dac.com/events/eventdetails.aspx?id=95-5-U - Cached - Similar

9. Setup and Hold **Timing Violations** Induced by Process Variations, in **...**

   by B Rebaud - 2008 - Cited by 1 - Related articles
   design of the **circuit** and its environmental conditions. Thus, design methodologies and CAD **...** Like **Static Timing** Analysis, two kinds of SSTA exist: **path**-based and block-based. **Path**-based SSTA **...** are generated from those **results**. SSTA outputs provide **..... corner** to take to be sure that no **violation** will appear. **...**
   ieeexplore.ieee.org/iel5/4556750/4556751/04556814.pdf?arnumber...

10. Methods for conserving memory in statistical **static timing** analysis

    This has led to considerable research into statistical **static timing** analysis **...** test slack or an early **mode** slack indicates a **timing** constraint **violation**. **...**
    www.freshpatents.com/-dt20090924ptan20090241078.php - Cached

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Web Results **1** - **10** of about **11,600** for **static timing circuit violation path results mode corner coverage report interface user input**. (**0.11** seconds)

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1. Applications in Class 716/6

An apparatus, program product and method perform **static timing** analysis on an **...** a canonical approximation of an **input** slew over a timing **path** to a first **corner** and. **...** MINIMUM TIMING **VIOLATION** CORRECTIONS IN AN INTEGRATED **CIRCUIT** DESIGN **...** through a logic gate using timing analysis **results** is described. **...**
www.freepatentsonline.com/ACC-716-6.html

2. **USER** TRACK - DAC Archives

We **report results** based on OCP benchmarks for a 672 processors with NOC multiprocessor. **.....** design with some blocks of partitions under MMMC (Multi-**Mode** Multi-**Corner**) condition. **.... Static Timing** Analysis of Single Track **Circuits ...** This verification flow enables timing-**violation**-driven ECO flows of large GasP **...**
www.dac.com/events/eventdetails.aspx?id=95-5-U - Cached - Similar

3. A Holistic Parallel and Hierarchical Approach towards Design-For-Test

by CP Ravikumar - All 4 versions
failures, or significant timing **violations** are noticed. Chip- **...** level ATPG **coverage reports**, timing **reports**, and formal **...** for **circuit** blocks, the effort involved in **static timing ....** "residual" **mode**, there is a **path** from SI to SO that spans **....** The basic **user interface** to the framework is through a **...**
doi.ieeecomputersociety.org/10.1109/ITC.2004.15

4. Test Generation in the Presence of **Timing** Exceptions and Constraints

by D Goswami - 2007 - Cited by 1 - Related articles
improved test **coverage** and test compression. The new method **... timing** exception **path** with setup **time violation** does not meet the setup **time** requirements. A **timing** exception **path** with **.....** For a **circuit** under test with N gates, the **static** analysis **...** configurable through a scan-**mode interface**. For each of these **...**
ieeexplore.ieee.org/.../04261271.pdf?...D... - Similar

5. **Static** Netlist Verification

number of vector sets is required to cover all the **corner** cases. Any change in the **.....** A graphical **user interface** (GUI) for easier debugging **.... results** from a given **input** without any timing **violations**. **... coverage**. **Static timing** analysis checks all the paths in the **circuit** or design, including the false paths. **...**
www.springerlink.com/index/r5g27651q1670ln6.pdf

6. [PDF] Three Facets of IBIS: **Interface**, Behavior and Measurement

File Format: PDF/Adobe Acrobat - View as HTML
Basic timing analysis. **Static timing** analysis: **Input** setup and hold time. **Static timing** analysis: Clock edge to **...** Allows for simulation **coverage** of the majority of nets on your **...** Simulate the data **path** for the rising and the falling edges **....** (external **circuit**) terminals to present the **results** of analysis **...**
www.vhdl.org/pub/ibis/summits/dec05/dodd.pdf - Similar

7. (SNUG 03 Item 15 **...**

May 14, 2003 **...** Synopsys owns 98.3% of the $26 million **static timing** analysis market. **...** set false **path**) it can take about 1/2 the load time again to re-calculate. **...** Even if you have to run the analysis in each **mode**/**corner** there should be summary **reports** that show all **violations** in the design in all **corners**. **...**
www.deepchip.com/items/snug03-15.html - Cached

8. [PDF] Implementing an End-to-End Low-Power Multi-Voltage Methodology

File Format: PDF/Adobe Acrobat - Quick View
ELS cells allow the **input** side of the domain **interface** to be shut off, while driving **..... Static timing** analysis is based on two delay components: the network delay and the cell delay. **...** Concurrent Multi-**Corner** and Multi-**Mode** (MCMM) Analysis and Optimization **...** As a **result**, the timing and constraint **reports ...**
www.synopsys.com/Solutions/EndSolutions/.../implement_wp.pdf

9. Accurate **timing** analysis of integrated **circuits** when combinatorial **...**

The accuracy of **timing** analysis of an integrated **circuit** is enhanced based on **...** for a weak process **corner**, setup **time violation** is of particular concern. **...** 4C depicts the current on **input path** corresponding to pin B. As may be easily **...** graphics controller 660, network **interface** 680, and **input interface** 690. **...**
www.freshpatents.com/Accurate-**timing**-analysis-of-integrated-**circuits**-when-combinatorial-logic-offers-a-load-dt20060202ptan20060026543.ph... - Cached

10. **Static Timing** Analysis for Nanometer Designs

Multi-**mode** multi-**corner** analysis, power management, **.....** Figure 3-11 Design modeled with **interface timing**. • **Input** sequential arc: This is described **.....** The **timing path report** can optionally include the expanded clock paths, **.....** Example with **Timing Violation** In this case, the data **path** delay is much larger **...**
www.scribd.com/**Static**-**Timing**-Analysis-for...Designs/.../22000607 - Cached

1 2 3 4 5 6 7 8 9 10 Next

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static timing mode corner timing violation percentage

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1. Chip Design » **Static Timing** Analysis at 28 nm: More and Bigger is **...**

   For over 10 years, design engineers have used the same **static timing** analysis **...** and distributed multi-**mode**/multi-**corner** (MM/MC) and location-based on-chip **...** game where an ECO that fixes the original **timing violation** creates another. **...**
   chipdesignmag.com/display.php?articleId=3790 - Cached

2. Embedded.com - Statistical **Static Timing** Analysis - A Better **...**

   Feb 3, 2009 **...** Statistical **static timing** analysis (SSTA) helps the design team to make **...** For example, the analysis at max Vdd and low temperature **corner** utilizes **...** only 0.5% of the manufactured parts will have a **timing violation**. **...**
   www.embedded.com › Design Articles - Cached

3. [PDF] **Timing** Yield Estimation Using Statistical **Static Timing** Analysis

   File Format: PDF/Adobe Acrobat - Quick View
   by M Pan - Cited by 7 - Related articles - All 7 versions
   by analyzing a circuit at multiple process **corners**. Although this method **.....** The **timing** yield when there is no set-up **time violations**. Circuits S38584 **...** only causes a few **percentage** of error on **timing** yield in small circuits, **...**
   www.eecs.northwestern.edu/~haizhou/publications/iscas05.pdf

4. METHOD TO IDENTIFY **TIMING VIOLATIONS** OUTSIDE OF MANUFACTURING **...**

   by NC Buck - 2009
   Sep 17, 2009 **...** One method of implementation is to use a multi-**corner static timing** analysis tool which calculates parameter sensitivities such as **...**
   www.freepatentsonline.com/y2009/0235217.html

5. METHOD TO IDENTIFY **TIMING VIOLATIONS** OUTSIDE OF MANUFACTURING **...**

   One method of implementation is to use a multi-**corner static timing** analysis **...** to focus on **timing violations** outside of the manufacturing spec limits. **...**
   www.faqs.org/patents/app/20090235217 - Cached

6. **STATIC TIMING** ANALYSIS

   by U PrimeTime
   Only a selected few timing reports relate to the real **timing violations**. **....** By analyzing the design at both **corners** of the operating conditions, a time- **....** the test-**mode** for **static timing** analysis. Case analysis for **...**
   www.springerlink.com/index/l328453k08637619.pdf - Similar

7. EETimes.com - Multi-**corner** multi-**mode** designs are no mean feat

   Apr 7, 2008 **...** From a multiple **corner** and **mode** context, the critical handicap of the **...** increase in SI-related **timing violations** due to increasing dominance of **...** What is needed is a built-in MCMM **static timing** analysis engine that **...**
   www.eetimes.com/showArticle.jhtml?articleID=207100049 - Cached - Similar

8. Magma - Quartz **Time**

   It provides the most sophisticated **static timing** and signal integrity analysis **...** Multi-**mode timing** analysis allows concurrent analysis and optimization of multiple **...** consuming to identify the single worst **corner**-case and to fix **violations**. Quartz **Time's** multi-**corner timing** analysis generates **timing** constraints **...**
   www.magma-da.com/products-solutions/analysis/quartz**time**.aspx - Cached

9. Incentia Announces ECOCraft, New Tool for Post-Layout Hold **Time** ECO

   Apr 29, 2008 **...** Fixing hold **time violations** under Multi-**Mode** Multi-**Corner** (MMMC) **...** Incentia patented technologies provide the fastest **Static Timing ...**
   www10.edacafe.com/nbc/articles/view_article.php?articleid=524145

10. The Missing **Corner** | Adventures on the Chip Design Road...

    Sep 28, 2009 **...** In test-**mode**, the clock will reach the clock-gate control flops much earlier than the **...** Looks like a hold-**time violation**. But why that **corner**? It's not one of the standard timing **corners** checked for tape-out. **...** that you'd need to run **static timing** analysis, you do analyze timing at the offending **...**
    chip101.com/blog/jmacdonald/2009/missing-**corner** - Cached

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static timing circuit (unanalyzed OR unprocessed OR unsimulated) results mode | Search | Advanced Search

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1. Test-Pattern Grading and Pattern Selection for Small-Delay Defects

   by M Yilmaz - 2008 - Cited by 3 - Related articles - All 3 versions

   [2, 6, 9]. However, the test generation time increases con- siderably when these tools are run in timing-aware **mode**. **...** using **static timing** analysis (STA) tools. Even with a list of **...** data volume and test application time for integrated **circuits ...** budget and target fault **coverage**. Experimental **results** show **...**

   ieeexplore.ieee.org/iel5/4511672/4511673/04511728.pdf?... - Similar

2. [PDF] MODELING OF DETERMINISTIC WITHIN-DIE VARIATION IN **TIMING** ANALYSIS **...**

   File Format: PDF/Adobe Acrobat - View as HTML

   by M Choi - 2007 - Cited by 1 - Related articles - All 10 versions

   are associated with increasing numbers of **unsimulated** features and design- **....** Most papers have focused on selecting paths to ensure topological **coverage**. **..... circuit**, which are in the bottom right **corner** of the chip in Figure 6.6(a). **.....** Figure 6.9 shows the delay **results** for **static timing** analysis of 10 **...**

   smartech.gatech.edu/bitstream/1853/.../1/choi_munkang_200705_phd.pdf

3. Image sensor **timing circuit** - Patent 7567279

   by ZA Yourlo - 2009

   Jul 28, 2009 **... Unprocessed**-Processed-Subsampled Image Read Sequence **.....** may be put in a bypass or transparent **mode** to increase **coverage** of signals going **...**

   www.freepatentsonline.com/7567279.html

4. [PDF] Test-Pattern Selection for Screening Small-Delay Defects in Very **...**

   File Format: PDF/Adobe Acrobat - View as HTML

   by M Yilmaz

   which induce small delay variations in the **circuit** components. Such delay variations are referred to as **...** and Encounter Test) or through a **static timing** analysis (STA) tool (for TetraMax). **.....** add **unprocessed** gates on the traced path to the stack **...** age as well as long-path **coverage**. As a **result**, we attempt to **...**

   dukespace.lib.duke.edu/dspace/.../Chakrabarty_duke_tech_report_2009.pdf

5. [PDF] System-on-Chip Testability Using LSSD Scan Structures

File Format: PDF/Adobe Acrobat - Quick View
by K Zarrineh - Cited by 9 - Related articles
design **time** to market for complex systems. Scan ..... which **results** in the **circuit** shown in Figure 8b. During functional **mode**, control ...
www.cse.buffalo.edu/~shambhu/documents/pdf/ieeednt01.pdf

6. Photodetecting **Circuit** - Patent application - is disclosed which ...

Timing diagram of the image sensor event signals in Freeze-Frame **mode** ..... either processed or **unprocessed**, to an external device using a serial data ...
www.faqs.org/patents/app/20100002111 - Cached

7. Scanning SQUID microscopy for current imaging - Elsevier

by LA Knauss - 2001 - Cited by 17 - Related articles - All 3 versions
During imaging, the MAGMA system achieves a raw, **unprocessed** spatial resolution equal ... A common failure **mode** in integrated **circuits** is the power to ground short. .... 14(a), the **static** magnetic field image is shown for the background magnetic ... Current image **results** overlaid on the **circuit** diagram for the MCM. ...
linkinghub.elsevier.com/retrieve/pii/S0026271401001081

8. Method of routing an integrated **circuit** - US Patent 6006024 ...

This step enhances tie **coverage** and performance of the final layout without ..... and a number of bends, or **corners** which **result** from the proposed layout. ...
www.patentstorm.us/patents/6006024/description.html

9. Wormlike Polystyrene Brushes in Thin Films - Langmuir (ACS ...

by SS Sheiko - 1997 - Cited by 72 - Related articles
Molecular ordering in thin films has been studied using tapping **mode** ... The incomplete **coverage results** from dewetting of the substrate during ... Figure 6 Fourier filtered (a, b) and **unprocessed** (c, d) SF micrographs of a ..... These brushes were characterized in solution (GPCMALLS, **static** and dynamic light . ...
pubs.acs.org/cgi-bin/jtext?langd5/13/i20/abs/la970132e

10. A survey of the Indian ocean triple junction trace within the ...

by P Patriat - 1989 - Cited by 7 - Related articles
processes at this **mode** of triple junctions appear to be supported .... single continuous lines; SEABEAM **coverage** is indicated by pale stipple or .... Crosses locate '**corner**' sections discussed in text, flagged bold lines are inward-facing scarps in ocean .... and to a lesser degree, of CIR and a **static** SEIR, the ...
www.springerlink.com/index/P366J0117923217 4.pdf

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static timing circuit merge results

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1. **Static Timing** Model Extraction for Combinational **Circuits**

   by B Li - Related articles
   For large **circuits**, **static timing** analysis (STA) needs to be **...** The serial **merge** replaces two consecutive timing edges by a new one from the **.....** Comparison of the Reduction **Results**. **Circuit**. Original **circuit**. Proposed method **...**
   www.springerlink.com/index/n61287m4wr624664.pdf

2. **STATIC timing** analysis of a digital **circuit** is a widely used

   by K Tseng - 2005 - Cited by 12 - Related articles
   The **results** from these designs and a few special **circuits** are presented in Section IV. II. **TIMING** ANALYSIS FRAMEWORK. In **static timing** analysis without **...**
   ieeexplore.ieee.org/iel5/43/32559/01522445.pdf?arnumber=1522445

3. NanoTime

   Transistor-level **Static Timing** Analysis Solution for Custom Designs **...** and delivers overnight analysis **results** for complex million-transistor designs. **...** Timing checks for complex **circuit** designs (domino logic, pass gates, **...** Ability to **merge** timing models; Industry-standard support, Liberty™, SDC, SPF, SPEF **...**
   www.synopsys.com/Tools/Implementation/.../Nano**Time**.aspx - Cached - Similar

4. Generation of refined switching windows in **static timing** analysis **...**

   The present invention generally relates to **circuit timing** analysis and more **.....** line shows the **results** of dividing the cycle **time** of the **circuit** into four equal **....** The process then returns to step 708 and continues to **merge** pairs of **...**
   www.patentstorm.us/patents/6651229/description.html

5. **[PDF]** Statistical **Static Timing** Analysis with Conditional Linear MAX/MIN **...**

   File Format: PDF/Adobe Acrobat - Quick View
   by L Zhang - Cited by 15 - Related articles - All 11 versions
   the MAX operator, with the understanding that the same **results** can be easily **..... circuit**. Each

repetition is a process of **static timing** analysis by fixing **...**
citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.74.8406&rep...

6. [PDF] Power Performance Optimization for Custom Digital **Circuits**

File Format: PDF/Adobe Acrobat - View as HTML
by R Zlatanovici - Cited by 10 - Related articles - All 9 versions
a convex optimization problem that **results** from the use of Elmore s formula for gate **...** Uses a **static timer** to perform all **circuit**,related computations, **.....** (R4) adders **merge** 4 carries at each stage, and therefore a 64,bit tree has **...**
www.eecs.berkeley.edu/~bora/publications/PATMOS05.pdf

7. [PDF] On Hierarchical Statistical **Static Timing** Analysis

File Format: PDF/Adobe Acrobat - Quick View
by B Li - Related articles - All 2 versions
the possibility of applying the basic **merge** operations is introduced in [13]. **.....** TABLE I. **RESULTS** OF **TIMING** MODEL EXTRACTION. **Circuit ...**
www.date-conference.com/archive/conference/proceedings/.../10.4_1.PDF

8. **Timing** Model Extraction of Hierarchical Blocks by Graph Reduction

by CW Moon
creating a **timing** model of a digital **circuit** for use with a **static timing** analyzer. **....** pins from a **timing** graph. Whenever s-**merge** is performed, arc **.....** Tables 2 and 3 present **results** of graph reduction on four industry designs. **...**
doi.ieeecomputersociety.org/10.1109/DAC.2002.1012611

9. **Timing** Model Extraction of Hierarchical Blocks by Graph Reduction

by CW Moon - 2002 - Cited by 17 - Related articles
creating a **timing** model of a digital **circuit** for use with a **static timing** analyzer. **...** behavior of the original **circuit** and produce accurate **results ....** s-**merge** takes two delay arcs (d1 and d2) in series and creates a new **...**
portal.acm.org/ft_gateway.cfm?id=513957&type=pdf

10. Ali Dasdan - Publications

A. Dasdan and S. Kolay, Search **Results** with Most Clicked Next Pages, Yahoo!, filed in 2008. **...** H.-C. Yang, A. Dasdan, and R.-L. Hsiao, Map-Reduce with **Merge** for **...** A. Dasdan and C. Aykanat, Two Novel **Circuit** Partitioning Algorithms Using **...** A. Dasdan, S. Kolay, and M. Yazgan, Derating in **Static Timing** Analysis: **...**
dasdan.net/ali/publications.php - Cached

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